A1 CONT

are switching at time T1 115, a delay is performed by delay logic 120. Delay logic 120 provides a sufficient delay to signal 2 105 in order to prevent simultaneous switching with signal 1 100 and/or signal 3 110. Signal 2 105 switches at time T2 125. The delay is a delay d 130. Delay d 130 can be a predetermined period of time or any amount of time sufficient to prevent simultaneous switching with signal 2 105 and adjacent signal 1 100 and signal 3 110. The delay avoids any coupling interference in the event that signal 2 105 is an opposite switching signal to either signal 1 100 and/or signal 3 110.

Please replace the paragraph on page 6, lines 5 – 19 with the following paragraph:

A2

Fig. 1E is a timing diagram illustrating a five-signal group with an extended delay when an initial delay results in simultaneously switching with an adjacent signal. In this particular embodiment of the invention, signal 2 105 and signal 4 135 are never delayed, and always switch at their respective original switch times, in this example signal 2 105 switches at time T1 115 and signal 4 135 switches at time T3 145. Signal 1 100, signal 3 110, and signal 5 140 switch at time T1 115, the same time that signal 2 105 switches. Delay logic 120 senses that adjacent signal 1 100 and signal 3 110 switch at the same time as signal 2 105, therefore a delay is provided to signal 1 100 and signal 3 110. Signal 1 100 now switches at time T3 145, the same time as signal 4 135, however the two signals are far enough removed from one another to avoid any coupling interference. Signal 3 110 would also be delayed to time T3 145, however, this condition would result in signal 3 110 switching at the same time as signal 4 135. Delay logic 120 therefore provides for signal 3 110 to be further delayed to time T5 155. The adjusted delayed timing diagram prevents adjacent signals from switching at the same times and avoids coupling interference when adjacent signals are switching opposite one another.

Please replace the paragraph on page 7, lines 7 – 14 with the following paragraph:

A3

Fig. 3 is a flow diagram illustrating transition of adjacent signals for a three signal group. Sensing and delay circuit 200 receives signals 100, 105, and 110, step 300. Signals 100 and 105 are sensed at the same time, step 305. Simultaneously, signals 105 and 110 are also sensed with one another at the same time, step 310. A determination is made if signals 100 and 105 are switching at the same time, step 315. A determination is also made whether signals 105 and 110 are switching at the same time, step 320. If the condition is "yes" for either steps 315 or 320, then signal 2 105 is delayed, step 325. If steps 315 and 320 are both determined to be "no," then signal 2 105 is not delayed, step 330.

Please replace the paragraph beginning on page 7 line 15 and ending on page 8 line 3 with the following paragraph:

A4

Fig. 4 is a block diagram illustrating use of a sensing and delay circuit and buffers to transition a five-signal group. Buffer 400 is used for signal 1 100. Buffer 405 is used for signal 2 105. Buffer 410 is used for signal 3 110. Buffer 415 is used for signal 4 135. Buffer 420 is used for signal 5 140. Buffers 400, 410, and 420 are tri-state buffers that receive delay signals from sensing and delay circuit 425. A received delay signal to the respective buffer tri-states the respective signals. In this particular example delay signal 430 is provided to buffer 420. Delay signal 435 is provided to buffer 410. Delay signal 440 is provided to buffer 400. Sensing and delay circuit 425, in this embodiment, includes three separate circuit or logic blocks: sensing and delay circuit A 445; sensing and delay circuit B 450; and sensing and delay circuit C 455. The respective sensing and delay circuits can include digital, analog, and/or combined circuits that sense and hold signals and trigger respective tri-state buffers 400, 405, 410, 415, and 420. In this particular embodiment, sensing and delay circuit A 445 senses signal 1 100 through sense signal